Register No : _____

THE KAVERY ENGINEERING COLLEGE

(An Autonomous Institution)

B.E/B.TECH DEGREE END SEMESTER THEORY EXAMINATIONS, APRIL/MAY 2025

Sixth Semester

Electronics and Communication Engineering

CEC334 - Analog IC Design

Regulations - 2021

Duration : 3 Hrs ***Maximum: 100 Marks***

PART – A (ANSWER ALL QUESTIONS) (Marks 10*2=20)

Q.No	*Questions*	*BLT*	*CO*	*Marks*
1.	Classify the different types of amplifier configurations in MOSFET circuits.	L2	1	2
2.	Name the key performance factors to be considered when designing a differential amplifier for high-speed applications.	L1	1	2
3.	Show how the Miller effect impacts the bandwidth of amplifiers.	L1	2	2
4.	List out the different types of noises associated with MOS devices.	L1	2	2
5.	State the effect of negative feedback on the bandwidth of an amplifier.	L1	3	2
6.	Define gain boosting.	L1	3	2
7.	State the need for compensation in a feedback amplifier.	L1	4	2
8.	Compare lock range and capture range.	L2	4	2
9.	List the types of detection and testing of faults.	L1	5	2
10.	Define Partial scan.	L1	5	2

PART – B (ANSWER ALL QUESTIONS) (Marks 5*16 = 80)

Q.No		*Questions*	*BLT*	*CO*	*Marks*
11.	a	Survey the CS, CG and Source follower circuits with required diagram in detail.	L4	1	16
		Or			
	b	Analyze the design of differential and cascode amplifiers with necessary diagrams.	L4	1	16
12.	a	Develop the frequency response of CS, CG and Source follower with required diagram in detail.	L3	2	16
		Or			

	b		Identify the statistical characteristics of noise with neat sketch.	L3	2	16
13.	a	i	Explain the properties and types of negative feedback circuits.	L2	3	9
		ii	Outline the operational amplifier performance parameters.	L2	3	7
			Or			
	b	i	Compare the single stage Op Amps, two-stage Op Amps.	L2	3	7
		ii	Summarize the noises in Op Amps.	L2	3	9
14.	a		Illustrate about the Multipole Systems with necessary diagrams.	L2	4	16
			Or			
	b		Summarize about slewing in two stage Op Amps and alternative method of compensation of two stage op-amp with neat diagrams.	L2	4	16
15.	a		Explain in detail about the faults in Logic Circuits.	L2	5	16
			Or			
	b		Illustrate the Built-in-Self-Test in detail with relevant diagrams.	L2	5	16